Remarks

The Official Action mailed September 20, 2005 rejected claims 2-3 and 5-21. Applicant has amended claims 12, 14-16 and 18-20, and added new claims 22-25. Claims 2-3 and 5-25 remain pending.

Claim Objections

Claims 14-15 and 18-19 were objected to for lack of spelling out the acronym IDE. Applicant has amended the claims 14-15 and 18-19 and the full form of the acronym IDE has been inserted in the claims. Applicant respectfully requests the objection be withdrawn.

Claim Rejections under 35 USC 103 (Baker/Runaldue)

The Official Action rejected claims 2-3, 5-21 as being unpatentable over Baker (US Parent 5,996,032) in view of Runaldue et al. (US Parent 5,999,441). Claim 20 has been amended. Applicant respectfully requests the rejection of claims 2-3, 5-21 be withdrawn.

Claims 2-3, 5-11 and 20-21

Claim 20, as amended requires receiving data of a write command comprising a bit enable field and a data field and each field comprises same number of bits.

Applicant is unable to locate where Baker teaches receiving data of a write command comprising a bit enable field and a data field comprises same number of bits in each field. The office action appears to rely upon figure 10 and the related description wherein Baker teaches a register write circuitry 250 for writing arbitrary

number of data bits. Register write circuitry 250 permits writing only to bits that must change in a register, while preserving the previous value of the remainder of bits.

Further Baker teaches that address field 272 includes GPIO register address bits 274 and individual select field 276 address bits $A_0 - A_3$, according to the bit value, 0 or 1, of the associated bits in address field 272. Baker thus does not appear teaching receiving data of a write command wherein the data comprises a bit enable field and a data field comprising same number of bits and then updating a register with one or more bits of the data field that are associated with enable bits of the bit enable bits and therefore Baker does not arrive at the invention of the applicant's claim 20.

Runaldue appears to teach a bit enabled decoder logic 18 to enable bit by bit writing using data bits and mask bits, but there is no indication that the mask bits are part of the data bits transmitted in a write command. Further, Runaldue appears to be silent regarding how exactly the mask bits are transmitted. Runaldue thus does not teach receiving data of a single write command wherein the data comprises a bit enable field and a data field having same number of bits in each field as required by the Applicant's claim 20.

Since the proposed combination of Baker and Runaldue does not teach receiving data of a write command comprising a bit enable field and a data field and updating a register with one or more bits of the data field comprises same number of bits and therefore the proposed combination does not arrive at the invention of Applicant's claims 20. Applicant respectfully requests the rejection of claim 20 be withdrawn.

If the Examiner elects to maintain the present rejection of claim 20, Applicant respectfully requests that the Examiner indicate with specificity (e.g. column and line)

where Baker and/or Runaldue teaches receiving data of a single write command wherein the data comprises a bit enable field and a data field having same number of bits in each bit enable field and data field.

Claims 2-3, 5-11 and 21 includes claim 20 as a base claim. Accordingly, claims 2-3, 5-11 and 21 are allowable for at least the reasons stated above in regard to claim 20. Additional points could be made in support of the allowance of claims 2-3, 5-11 and 21. However, Applicant believes the above is sufficient to overcome the present rejection of claims 2-3, 5-11 and 21 under Baker. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with the review of superfluous points. Applicant respectfully requests that the rejection of claims 2-3, 5-11 and 21 be withdrawn.

Claims 12 – 15

Claim 12 as amended, requires receiving a data value of a write directed to a control register and interpreting bits of the data value as a data field and bits of the data value as an enable field.

Baker in (column 10, lines 60 – column 11 lines 20) teaches that the link layer control and status register 92 includes DMA channel 4-0 word 0 packet compare value register and each register is assigned to DMA channel comparator logic function. The DMA channel comparator matches a select set of bit positions in the compare value register, to corresponding bit positions of the first quadlet (word 0) of the incoming packet. The bit positions to match are specified by the mask value contained in the word 0 receive packet compare mask register. A DMA channel 4-0 ward 0 receive packet compare mask register is assigned to a corresponding DMA channel comparator. Applicant is unable to locate where Baker teaches receiving a

data value of a write directed to a control register and interpreting bits of the data value as a data field and bits of the data value as an enable field.

Runaldue in the cited columns and lines teaches an arrangement for enabling data to be written in an addressed word in memory on bit-by-bit basis. Runaldue as well as Baker, however does not appear to teach receiving a data value of a write directed to a control register and interpreting bits of the data value as data field and bits of the data value as an enable field.

Since the proposed combination of Baker and Runaldue does not teach each and every element of Applicant's claim 12, the proposed combination does not arrive at the invention of Applicant's claim 12. Applicant respectfully requests the rejection of claim 12 be withdrawn.

If the Examiner elects to maintain the present rejection of claim 12, Applicant respectfully requests that the Examiner indicate with specificity (e.g. column and line) where Baker and/or Runaldue teaches receiving a data value of a write directed to a control register and interpreting bits of the data value as a data field and bits of the data value as an enable field.

Claims 13-15 include claim 12 as a base claim. Accordingly, claims 13-15 are allowable for at least the reasons stated above in regard to claim 12. Additional points could be made in support of the allowance of claims 13-15. However, Applicant believes the above is sufficient to overcome the present rejection of claims 13-15 under Baker. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with the review of superfluous points. Applicant respectfully requests that the rejection of claims 13-15 be withdrawn.

Claims 16 – 19

Claim 16, as amended, requires overwriting only the bits at the bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value.

The office action appears to rely upon the same rational of rejection as applicable in case of claim 12. Applicant, as submitted with regard to claim 12 herein above, submits that applicant is unable to locate where Baker teaches overwriting only the bits at the bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value.

Runaldue in the cited columns and lines teaches regarding need for an arrangement for enabling data to be written in an addressed word in memory on bit-by-bit basis.

Baker as well as Runaldue however does not provide teaching overwriting only the bits at the bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value.

Since the proposed combination of Baker and Runaldue does not teach each and every element of Applicant's claim 16, the proposed combination does not arrive at the invention of Applicant's claim 16. Applicant respectfully requests the rejection of claim 16 be withdrawn.

If the Examiner elects to maintain the present rejection of claim 16, Applicant respectfully requests that the Examiner indicate with specificity (e.g. column and line) where Baker and/or Runaldue teaches overwriting only the bits at the bit locations of the register for which the enable bit in the corresponding locations in the bit enable field is set with the bits in the corresponding location in the data field.

Claims 17-19 include claim 16 as a base claim. Accordingly, claims 17-19 are allowable for at least the reasons stated above in regard to claim 16. Additional points could be made in support of the allowance of claims 17-19. However, Applicant believes the above is sufficient to overcome the present rejection of claims 17-19 under Baker. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with the review of superfluous points. Applicant respectfully requests that the rejection of claims 17-19 be withdrawn.

Newly Added Claims

Applicant has added new claims 22-25 which include novel and non-obvious limitations. Applicant submits that neither Baker nor Runaldue teaches the limitations of the newly added claims. Applicant respectfully requests allowance of claim 22-25.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that all remaining claims are in condition for allowance. Reconsideration is requested, and allowance of all remaining claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

Date: December 19, 2005

Gregory D. Caldwell
Reg. No. 39,926

Blakely, Sokoloff, Taylor & Zafman, LLP
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
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On: December 19, 2005

Signature: Katherine Jennings